Çok Çıkışlı Flyback Dönüştürücüde Çıkış Geriliminin Yüke Bağlı İncelenmesi

Araştırma Makalesi / Research Article

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ÖZ

Günümüz anahtarlamalı güç kaynakları güvenirliği ve yüksek verimliliğiden dolayı tercih edilmektedir. Birçok anahtarlamaları güç kaynağı topolojisi vardır. Bu topolojilerden birisi de izalasyonun sağlanıp ve çok çıkışın elde edilebilmesinden dolayı flyback dönüştürücüdür. Tezin bölümlerinde çok çıkışlı flyback dönüştürücü topolojisi anlatılıp örnek bir sistemi matematiksel bağıntıları verilip bilgisayar ortamında modellenmiştir. Bilgisayar ortamında tasarlanan bu model trafodaki yüksüz bir sargıdan geri besleme işareti oranlanıp kontrol devresine verilmektedir. Kontrol devresinden elde edilen kapı sinyali elektronik anahtarı yüksek frekansta tetikleyip çıkış gerilimlerini ayarlamaktadır. Ancak geri besleme işareti tek bir sargıdan alındığından alınan sargının gerilimi istenen değerde tutulmasına rağmen, trafodaki ortak endüktans etkisinden dolayı diğer gerilimlerde yük durumlarına göre ve ya giriş gerilimleri değişimleri sonucu çıkış gerilimlerinde değişimler meydana gelmektedir. Bu değişimleri gösterebilmek için ORCAD 16.6 programından yararlanılıp öngörülen modelin çalışması yapılmıştır.

Anahtar Kelimeler: Çok çıkışlı flyback dönüştürücü, psipice.

Investigation of Output Voltages Depending On Load In Multi Output Flyback Converter

ABSTRACT

Switched mode power supplies (SMPS) is currently preferred due to safety and high efficiency. Flyback converter, which is one of topologies used by various switches, is capable of providing voltage isolation and multioutput. This article firstly attempts to investigate the topology of multioutput flyback converter, and then to model it in a computer based simulation utilizing from mathematical analysis. This simulation based modelling is designed to control the integrated circuit (IC) by getting ratio a voltage from unloaded feedback winding. Gate pulse providing from control circuit regulate output voltages by triggering MOSFET. The feedback signal is taken from one of the windings to perform good efficiency and best cost. Although the feedback winding is at desired voltage, other output is to change according to load conditions in outputs or to input voltages, because of mutual inductance and other condition. To represent the variables in the design of a flyback power supply with six isolated output, the model have been run properly on ORCAD 16.6 by showing the transient and steady state simulations of converter. Unlike other simulation programs, this model is fully designed for all nonlinear components without using blocks.

Keywords: Multioutput flyback converter, psipice

1. INTRODUCTION

Today, there are many switching power supplies which widely used in industry due to fast switching response and high stability. Various topologies have been emerged in switching power supplies due to problems of insulation and multioutput. The flyback converters is one of switching power supplies providing multioutput energy storage, insulation and voltage transformation via transformer and also output voltages up to 5000V can be obtained [1-2]. Moreover, when compared to other topologies, flyback converter topology can be used both buck type and boost type in extensive output voltage range [3]. In the many studies [4-6], flyback converters have been designed using opto-coupler for the purpose of isolation. Although an opto-coupler offers easy way to capture the output voltage, its transfer function is nonlinear, dependent on ambient temperature, to occur time delay and to change its characteristic as a depending on production. These drawbacks impose efficiency and quality of converter circuit [7, 8]. In this article, flyback primary-side control was adopted to control the flyback converter in discontinuous conduction mode (DCM) to perform stable performance. The simulation of a flyback power supply with six isolated output with different voltage levels have been examined and compared with loading and input varieties. Besides, this simulation is close to the truth, unlike many of simulation worked on this converter. In this design, it has been benefit from technical documents [9-16].

2. DESCRIPTION OF THE MULTI OUTPUT FLYBACK CONVERTER

The schematic diagram of a multi output Flyback converter is shown in fig 1. Energy is stored in the

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magnetic circuit when the switch is turned on and the stored energy is discharged and transferred to the load during off period of the switch.

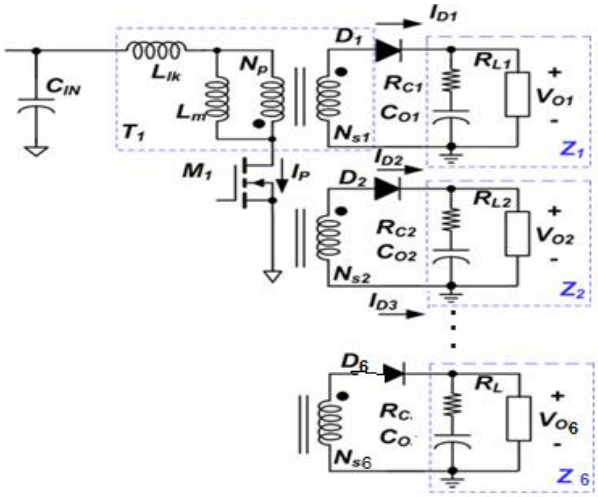

Figure 1. Schematic diagram of multioutput flyback converter.

The specifications and considerations made during design of the converter are explained in the following steps:

2.1. The System Specifications

The converter supplies six independent loads with the rated voltages and currents as: i- 3.3V, 1A, ii- + 5V, 1A, iii- -5V, 250mA, iv- + 15V, 250mA, v- -15V, 250mA, vi- + 25V, 200mA. The line frequency is 50Hz and the line voltage is considered to be in the range of 85 to 265 V. During design the efficiency of the converter (E_{ff}) will be also considered as a criteria such that not to be less than 80%. Maximum output power is given as Po. The maximum input power (P_{in}) is defined in equation 1.

$$P_{in}=\frac{P_O}{E_{ff}} \quad (1)$$

For multiple output switching mode power supplies (SMPS), the load occupying factor for each output $K_{L(n)}$ for the n-th output is defined as given in equation 2 and Po(n) is the maximum output power for the n-th output. For single output SMPS, $K_{L(1)}=1$.

$$K_{L(n)}=\frac{P_{O(n)}}{P_O} \quad (2)$$

2.2. Determining DC Link Capacitor and The DC Link Voltage Range

The typical value of the DC link capacitor value is as 2-3µF per watt of input power. In this study, the value of C_{in} is selected as 47µF and flyback converter has input voltage range of $85V_{rms}$ - 265Vrms. We may use equations 3 to obtain minimum DC link voltage.

$$V_{DC}^{min}=\sqrt{2\,(V_{line}^{min})^2-\frac{P_{in}\,(1-D_{ch})}{f_L\;C_{in}}}=71V \quad (3)$$

Where D_{ch} is the DC link capacitor charging duty ratio, which is typically about 0.2 because of DC link voltage waveform of single phase. Line frequency (f_L), minimum line voltage (V_{line}^{min}) is respectively 50 Hz, 85Vrms. Maximum line voltage (V_{line}^{max}) is selected 265Vrms. The maximum DC link voltage is derived using equation 4.

$$V_{DC}^{max}=\sqrt{2}\,V_{line}^{max}=375V \quad (4)$$

2.3. Determining The Maximum Duty Ratio (Dmax)

D_{max} is approximately in the range of 0.45~0.5 for universal input range application. When the MOSFET is turned off, the input voltage (V_{DC}) together with the output voltage reflected to the primary (V_{RO}) are imposed on the MOSFET. In this study, the maximum duty ratio (D_{max}) has been chosen as 0,485. The value of V_{RO} and voltage between drain and source terminals of MOSFET (V_{ds}^{nom}) are determined using equations 5 and 6.

$$V_{RO}=\frac{D_{max}}{1-D_{max}}\,.\,V_{DC}^{min}=67V \quad (5)$$

$$V_{ds}^{nom}=V_{DC}^{max}+V_{RO}=442V \quad (6)$$

2.4. Determining The Transformer Primary Side Inductance (L_m)

In most of the flyback converter, its operation changes between continuous conduction mode (CCM) and DCM as depending the load condition and input voltage. For both operation modes, considering the worst case in designing, the inductance of the transformer primary side (L_m) is adopted full load and minimum input voltage condition. Therefore, L_m is obtained using equation 7 and f_s is the switching frequency.

$$L_m=\frac{(V_{DC}^{min}\,.\,D_{max})^2}{2\,P_{in}f_sK_{RF}}=333\mu H \quad (7)$$

When the flyback converter is operating in CCM, it is appropriate to set KRF = 0.25-0.5 for the universal input range and KRF = 0.4-0.8 for the European input range. In this study, KRF is chosen as 1 for DCM because of non-subharmonics. After determining of L_m, the maximum peak current (I_{ds}^{peak}) of the MOSFET in normal operation can be obtained from equation 8.

$$I_{ds}^{peak}=\frac{P_{in}}{V_{DC}^{min}D_{max}}+\frac{V_{DC}^{min}D_{max}}{2\,L_mf_s}=1.6A \quad (8)$$

2.5. Determining The Proper Core and The Minimum Primary Turns

Considering the core Etd 3C90, the minimum number of turns for the transformer primary side (N_P^{min}) to avoid the core saturation is given by equation 9.

$$N_P^{min}=\frac{1.12\,L_m\,I_{ds}^{peak}}{B_{sat}\,A_e}x10^6=17.7\text{ Turn} \quad (9)$$

where B_{sat} is the saturation flux density in tesla and approximately 0,3, A_e is the cross-sectional area of the core.

2.6. Determining The Number of Turns For Each Output

The turns ratio (n) between the primary side and first secondary winding

$$n=\frac{N_P}{N_{S1}}=\frac{V_{RO}}{V_{F1}+V_{O1}}=\frac{67}{3,3+0,5}=\frac{N_P}{3}\rightarrow N_P\cong 53\text{ Turn} \quad (10)$$

with Etd39_3C90 chosen the gap length of the core is calculated with equation 11.

$$G = 40\pi A_e\left(\frac{N_P{}^2}{1000\,L_m} - \frac{1}{A_L}\right) \cong 1.263\text{mm} \quad (11)$$

where A_L is the A_L-value with no gap in nH/turns^2 and it is chosen 2700 nH/turns^2 for Etd39_3C90 core examining datasheet. Using equation 10 for each winding, shown as winding turn numbers in table 1. All values are chosen approximate due to designing problem.

Table 1. Calculated winding turn number

Winding	Voltage value (V)	Winding turn number
Secondary1	+3.3	3
Secondary2	+5	4.5
Secondary3	-5	4.5
Secondary4	+15	12
Secondary5	-15	12
Secondary6	+25	20
Auxiliary winding	+15	12

2.7. Determining The Diameters of Conductors

The rms current of the n-th secondary winding is obtained using equation 12. The diameters of different windings are derived considering their current and theirs values are given in Table 2.

$$I_{sec(n)}{}^{rms} = I_{ds}{}^{rms}\sqrt{\frac{(1-D_{max})}{D_{max}}\frac{V_{RO}K_{L(n)}}{(V_{o(n)}+V_{F(n)})}} \quad (12)$$

where $V_{F(n)}$ is the diode $D_{R(n)}$ forward voltage.

Table 2. Diameters of the conductors of the windings

Winding	RMS Current value (A)	Wire diameter (mm)
Primary	0.6	0.405
Secondary1	1.7	3.264
Secondary2	1.8	2.588
Secondary3	0.5	2.588
Secondary4	0.5	1.291
Secondary5	0.5	1.291
Secondary6	0.4	1.024
Auxiliary winding	0.1	1.291

2.8. Choosing The Output Diodes and Capacitors

The maximum reverse voltage ($V_{D(n)}$) and the rms current of the rectifier diode $D_{R(n)}$ of the n-th output ($I_{D(n)}{}^{rms}$) are obtained using equation 13 and 14.

$$V_{D(n)} = V_{o(n)} + \frac{V_{DC}{}^{max}(V_{O(n)}+V_{F(n)})}{V_{RO}} \quad (13)$$

$$I_{D(n)}{}^{rms} = I_{ds}{}^{rms}\sqrt{\frac{1-D_{max}}{D_{max}}\frac{V_{RO}K_{L(n)}}{V_{o(n)}+V_{F(n)}}} \quad (14)$$

V_{RRM} is the maximum reverse voltage and I_F the average forward current of the diode and their values are determined using equation 15 and 16, respectively.

$$V_{RRM} > 1.3\,V_{D(n)} \quad (15)$$

$$I_F > 1.5\,I_{D(n)}{}^{rms} \quad (16)$$

The voltage and current ripple values of the n-th output capacitor are obtained from equation 17 and 18 respectively and appropriately are consisted of table 3.

$$\Delta V_{O(n)} = \frac{D_{max}\,I_{O(n)}}{f_s\,C_{o(n)}} + \frac{K_{L(n)}\,R_{C(n)}V_{RO}\,I_{ds}{}^{peak}}{(V_{o(n)}+V_{F(n)})} \quad (17)$$

$$I_{cap(n)}{}^{rms} = \sqrt{(I_{D(n)}{}^{rms})^2 - I_{o(n)}{}^2} \quad (18)$$

2.9. Designing The Snubber Circuit Parameters

When the power MOSFET is turned off, there is a high voltage spike between drain and source terminals due to existence of the transformer leakage inductance. This excessive voltage on the MOSFET may lead to failure of MOSFET. Therefore, it is essential to use an additional circuit to limit this spike voltage. The power dissipated in the snubber circuit (P_{sn}) is determined using equation 19.

$$P_{sn} = \frac{V_{sn}{}^2}{R_{sn}} = \frac{1}{2}f_s L_{lK}(I_{ds}{}^{peak})^2\frac{V_{sn}}{V_{sn}-V_{RO}} \cong 0{,}8\text{W} \quad (19)$$

V_{sn} is the snubber capacitor voltage at the minimum input voltage and full load condition, L_{lk} is the leakage inductance, V_{RO} is the reflected output voltage and R_{sn} is the snubber resistor. V_{sn} should be larger than V_{RO} and it is typical to set Vsn to be 2~2.5 times of V_{RO}.

Using equation (19) R_{sn} is obtained as 33.8 kΩ.

The maximum ripple of the snubber capacitor voltage is calculated using equation 20.

$$\Delta V_{sn} = \frac{V_{sn1}}{C_{sn}R_{sn}f_s} \rightarrow C_{sn} = \frac{V_{sn1}}{\Delta V_{sn}R_{sn}f_s} \cong 4{,}5\text{nF} \quad (20)$$

2.10. Designing The Control Parameters

The bode plot is an important tool for stability analysis of closed loop systems. It is based on calculating the amplitude and phase angle for transfer function. In section 2.10, flyback converter will be analysed with bode plots using MATLAB.

A system with feedback control is illustrated with the flow diagram of figure 2. Our system is same as this control system. The control-to-output transfer function

Table 3. The calculated values of output capacitors and value of rectifier diode

Output (V)	Capacitors value (μF)	$I_{cap(n)}$ (A)	$\Delta V_{O(n)}$ (V)	Type of diode	$I_{D(n)}{}^{rms}$ (A)	$V_{D(n)}$ (V)
+3.3	2200	1.4	0.18	MBR340	1.75	25
+5	2200	1.5	0.19	MBR360	1.83	36
-5	470	0.4	0.07	MBRS420	0.46	36
+15	470	0.4	0.07	MBRS420	0.49	102
-15	470	0.4	0.07	MBRS420	0.49	102
+25	470	0.3	0.06	MBR40250	0.39	168

of the Flyback converter or Power Stage '$H_{(s)}$' and compensation network '$C_{(s)}$' is defined in figure 2.

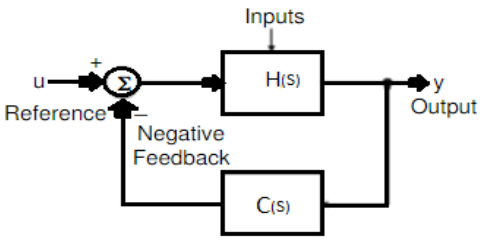

Figure 2. The Flyback with feedback control

Closed loop transfer function is derived from equation 21 [13].

$$T_{(s)}=\frac{H(s)}{1+H(s)G(s)} \quad (21)$$

For DCM operation, the Flyback converters' Power Stage ($H_{(s)}$) with current mode control is given by equation 22.

$$H_{(s)}= K\,\frac{1+\frac{s}{wz}}{1+\frac{s}{wp}} \quad (22)$$

K can be calculated using equation 23.

$$K = \frac{R_L(1-D_{max})}{n_{aux}\,R_{cs}\,A_v\,(1+D_{max})}= 8{,}33 \quad (23)$$

where voltage gain (Av) is 3 for SG1842

Sense resistance (R_{cs}), total effective resistance (R_L), turn ratio (n_{aux}) are determined using equation 24, 25 and 26 respectively.

$$R_{cs}=\frac{1.0V}{I_{ds(max)}} = 0{,}625\Omega \quad (24)$$

$$R_L = \frac{Vo^2}{Po} = \frac{15^2}{22{,}05} = 10{,}2\Omega \quad (25)$$

$$n_{aux}= \frac{N_{aux}}{N_p} =\frac{12}{53} = 0{,}226 \quad (26)$$

In our converter, Co = 40µF, r_c =100mΩ for aux is determined. Poles and zeros is given respectively by equation 27, 28.

$$w_z = \frac{1}{r_c C_O} = 250000 \text{ (rad/sn)} \quad (27)$$

$$w_p = \frac{2}{R_L C_O} = 4900 \text{ (rad/sn)} \quad (28)$$

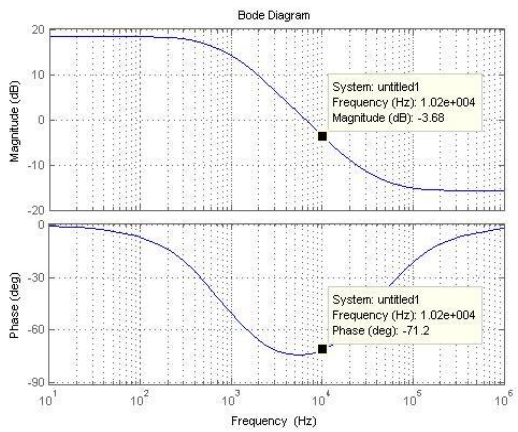

Figure 3. Transfer function of power stage

Figure 3 shows the transfer function of power stage for our example Flyback converter. One can see the poles and zeros and the DC gain as calculated. We need stability for flyback converter. Thus, it has been determinated crossover frequency (f_c). There are three conditions to define f_c.

-Right-half-plane zero (RHP) zero crossover limit
-Switching frequency crossover limit
-Capacitor esr crossover limit

It is not important to examine RHP zero crossover limit for DCM flyback due to high frequency. Crossover frequency is theoretically enough half of switching frequency according to Nyquist, but noise becomes an issue in SMPS at this frequency. Thus, this frequency is obtained with equation 29 in reality.

$$f_c \le \frac{f_s}{5} \quad (29)$$

Other crossover limit is capacitor esr crossover limit. If SMPS is driven by step loading, this limit is unimportant. Esr crossover limit is calculated using equation 30.

$$f_c \le \frac{1}{2\pi\, C\, r_c} \quad (30)$$

In our design, switching frequency crossover limit and capacitor esr crossover limit is calculated respectively 13kHz, 39,8kHz using equation 29 and 30. Thus, crossover frequency (f_c) is selected 10,2kHz. At this crossover frequency, power stage (H(s)) is calculated -3,68 DB and -71,2°. Thus, we need to a compensation network. Compensation network is a transfer function which gives one poles. R_b, which is shown in fig 5, doesn't play any role in the transfer function, but is needed to regulate the output steady-state voltage. (adjusting 2,5V to pin 2)

$$C_{(s)}= \frac{Ra}{Rc\,(1+s\,Ca\,Ra)} \quad (31)$$

R_a = 150kΩ, R_b = 4kΩ, C_a = 500pF, R_c = 20kΩ as shown in figure 5.

In order to view stability of Flyback converter, we have to know loop transfer function of this system. It can be obtained with equation 32 [14].

$$L(s) = H(s)\,C(s) \quad (32)$$

Loop transfer function is plotted using equation 31 in figure 4. According to the Nyquist criterion, if the loop gain is at 0 dB and the phase lag at crossover frequency is less than 180°, the system is stable. The phase margin (PM) is the difference between the phase and 180° [15]. However, while a control circuit has been designed, it should not be forgotten that loop transfer function with 30° or less phase margin has a tendency to occurring ring. On the other hand, this systems has fast response [16].

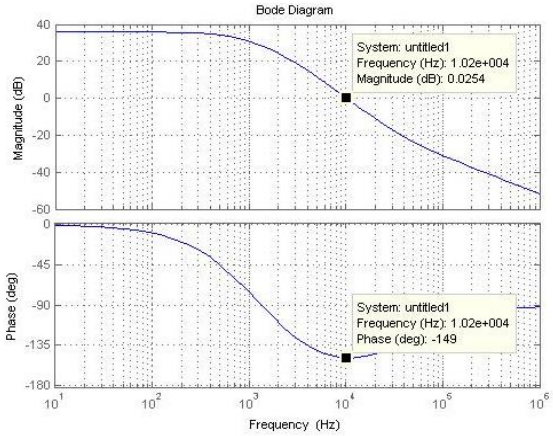

Figure 4. Loop transfer function of flyback converter

In our flyback, loop transfer function of flyback is calculated P.M= 31° at crossover frequency which is 10,2 kHz. Thus, it is observed that the designed system is stable. In addition to this, since the compensation network with the supply winding is provided in here, both the insulation problem and the nonlinear element (opto-couplor) have been eliminated. In this way, efficiency is increased and cost is reduced.

3. SIMULATION RESULTS

d In this simulation study, Orcad Pspice 16.6 program have been used by taking care of eight-winding mutual inductance. Coupling factor (k) is 0,992 between all winding. '85-265 V_{AC}' (universal input) can be used as the input source. Current mode control method has been applied. Thus, IC control has been selected SG1842 in simulation. Besides, Start-up Circuit has been designed to examine transient-state. RCD snubber used parallel to switch because of leakage inuctance. All the circuit components which is nonlinear are used as designed in the design example in figure 5.

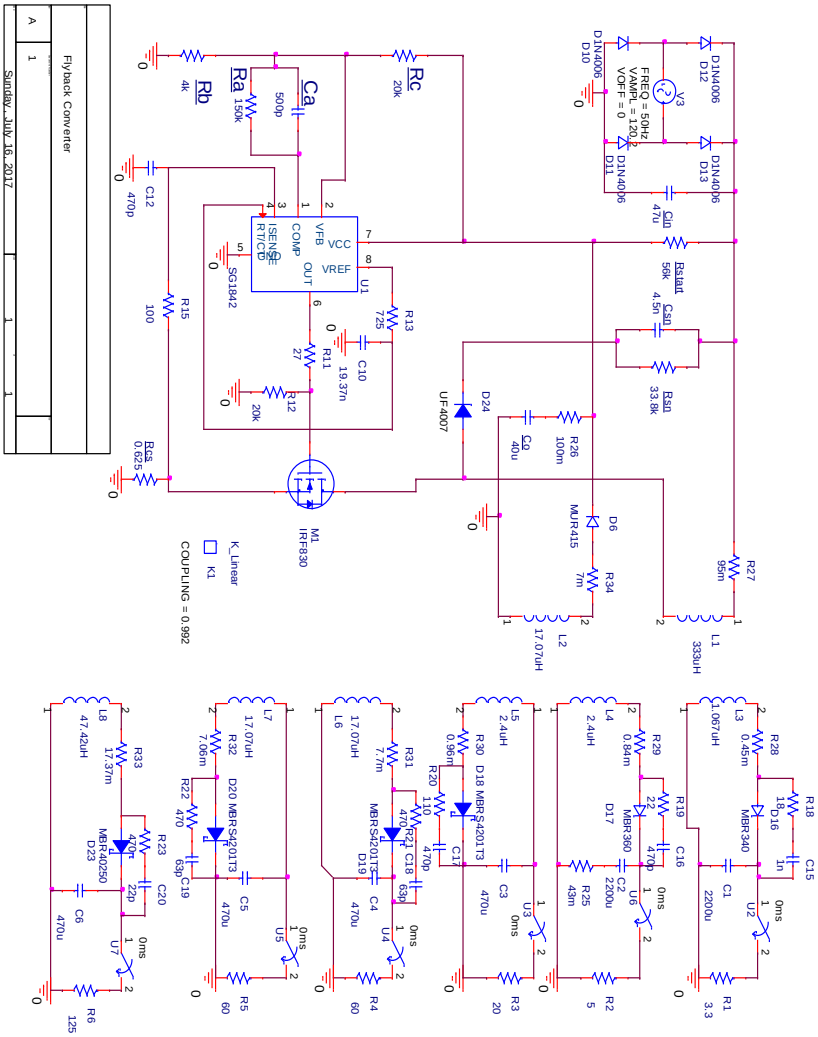

Figure 5. Simulated flyback converter

Table 5. Changing output voltage to loading at input voltage 220V rms

Unloading Winding	Load(%)	Vo1 (3.3V)	Vo2 (5V)	Vo3 (-5V)	Vo4 (15V)	Vo5 (-15V)	Vo6 (25V)
–	100	3.342	5.131	-5.092	14.634	-14.634	24.986
		1.28%	2.61%	1.84%	-2.44%	-2.44%	-0.06%
1,3	79,37	3.754	5.075	-5.542	14.559	-14.559	24.868
		13.75%	1.50%	10.83%	-2.94%	-2.94%	-0.53%
3,4,5	60,31	3.325	5.147	-5.559	15.422	-15.422	25.032
		0.75%	2.94%	11.17%	2.81%	2.81%	0.13%
1,2,6	39,68	3.731	5.611	-5.105	14.688	-14.689	26.640
		13.06%	12.21%	2.09%	-2.08%	-2.07%	6.56%
2,4,5,6	20,63	3.304	5.614	-5.132	15.354	-15.354	26.585
		0.12%	12.28%	2.63%	2.36%	2.36%	6.34%
1,2,3,4,5,6	0	3.733	5.630	-5.521	15.423	-15.423	26.164
		13.12%	12.61%	10.43%	2.82%	2.82%	4.66%

Table 6.Output powers based on percentage load changes at Vin 220Vrms.

Unloading Winding	Loading percentage (%)	Po_1(w)	Po_2(w)	Po_3(w)	Po_4(w)	Po_5(w)	Po_6(w)	P_{total}(W)
-	100	3.3851	5.26441	1.2964	3.5692	3.5692	4.9944	22.0788
1,3	79,37	0	5.15113	0	3.5327	3.5327	4.9473	17.1639
3,4,5	60,31	3.3496	5.29832	0	0	0	5.0128	13.6607
1,2,6	39,68	0	0	1.3028	3.5956	3.5961	0	8.49453
2,4,5,6	20,63	3.3076	0	1.3167	0	0	0	4.62432
1,2,3,4,5,6	0	0	0	0	0	0	0	0

Table 7. Output voltages according to input voltage changes at full load

Vin	Vo1 (3.3V)	Vo2 (5V)	Vo3 (-5V)	Vo4 (15V)	Vo5 (-15V)	Vo6 (25V)
85Vac	3.32	5.0482	-5.0531	14.526	-14.527	24.761
	0.61%	0.96%	1.06%	-3.16%	-3.15%	-0.96%
130Vac	3.3227	5.0591	-5.0648	14.561	-14.561	24.832
	0.69%	1.18%	1.30%	-2.93%	-2.93%	-0.67%
175Vac	3.3397	5.1261	-5.0875	14.62	-14.621	24.951
	1.20%	2.52%	1.75%	-2.53%	-2.53%	-0.20%
220Vac	3.3423	5.1305	-5.0919	14.634	-14.634	24.986
	1.28%	2.61%	1.84%	-2.44%	-2.44%	-0.06%
265Vac	3.3427	5.1311	-5.0924	14.635	-14.636	24.997
	1.29%	2.62%	1.85%	-2.43%	-2.43%	-0.01%

Table 5 shows the changes in the output voltages of the designed flyback converter with load changes. The output voltages change due to the mutual inductance between the windings. The changes in voltage on the windings do not exceed 15 percent of their nominal voltages. Table 6 shows output powers based on percentage load changes at Vin 220Vrms. The Flyback converter operates as a stable system at the output load changes. Output voltages are given according to the input voltage changes of the designed flyback converter in table 7. The increase in the input voltage of the designed model is observed to increase slightly in the output voltage

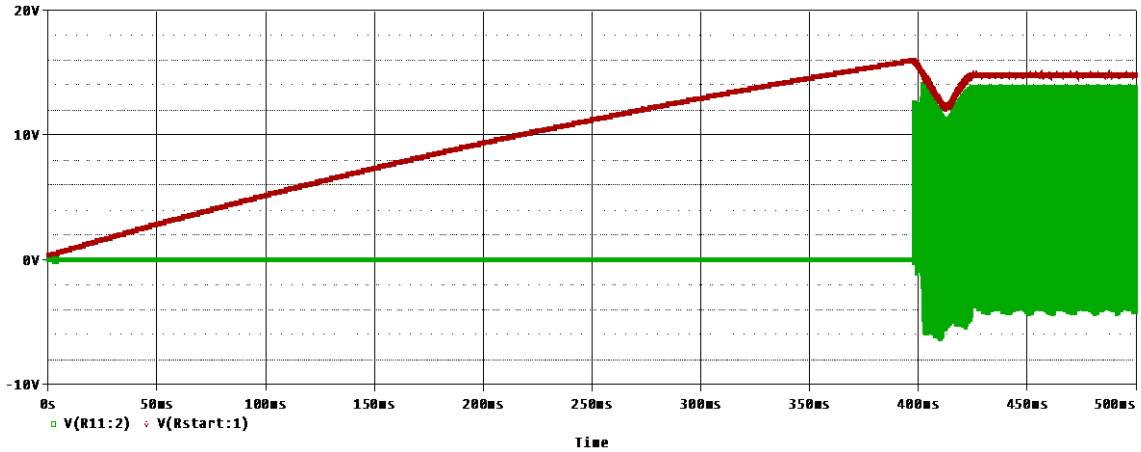

Figure 6. Bulk capacitor voltage at input voltage 85Vrms using full load

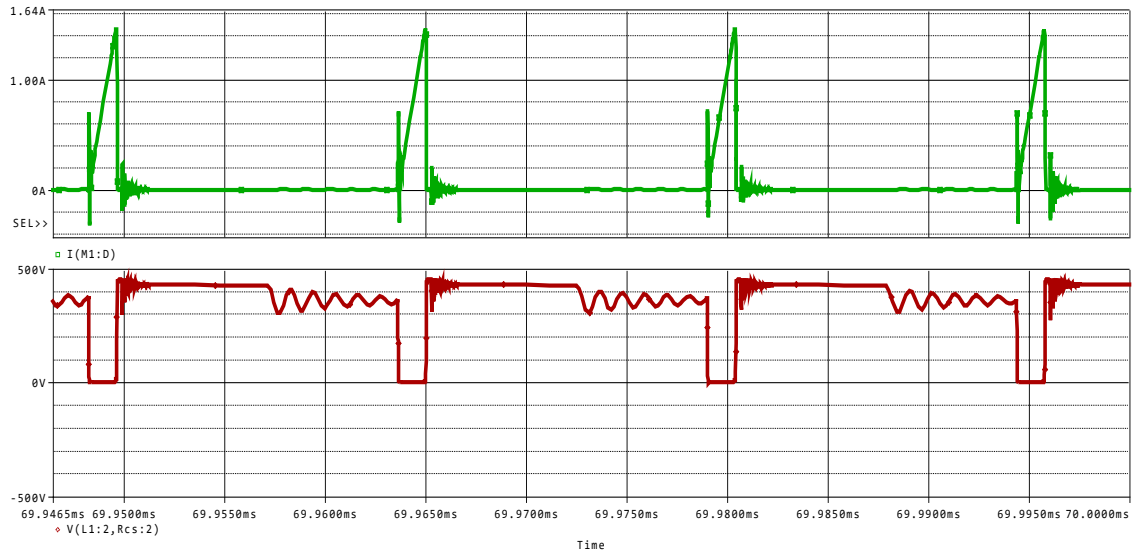

Figure 7. Waveforms of drain current and voltage at 265Vac and full load condition

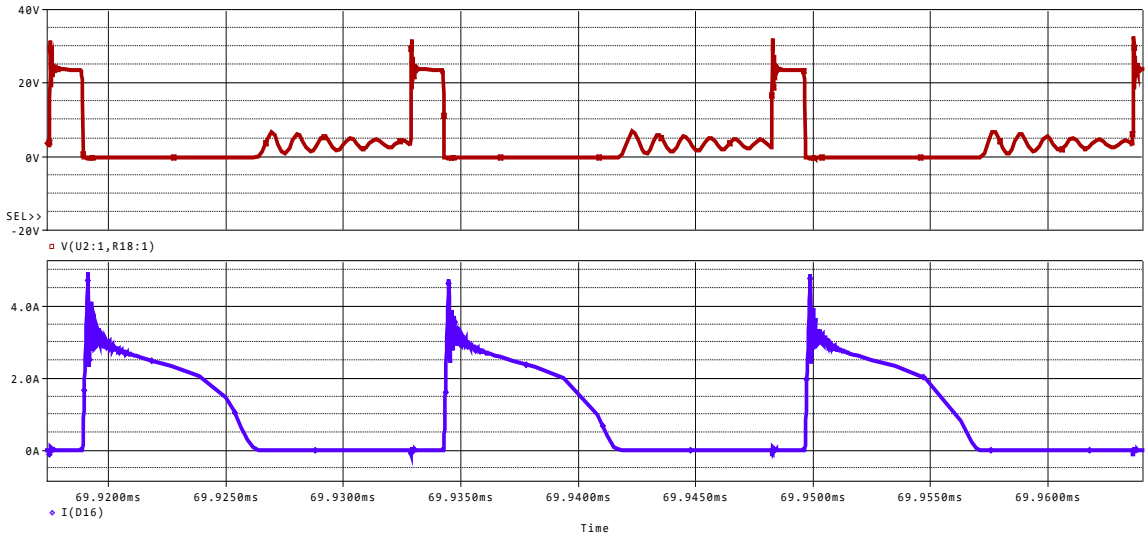

Figure 8. Current and voltage waveforms of the first output (3.3V) rectifier diode at 265Vac and full load condition

The bulk capacitor is to provide enough energy to prevent its voltage from dropping below the UVLO-off threshold during start-up. It is given cycle between 10-16V bulk voltage to run SG1842. It is shouldn't be forgotten that when Vbulk firstly become 17V, SG1842 will run in this range. Thus, the aux output voltage is taken 15V in this converter. The aux winding output (bulk voltage) is to reach its regulated level in figure 6. Figure 7 shows the FPS drain current and voltage waveforms at the maximum input voltage and full load condition. The maximum voltage stress on the MOSFET is about 450V, which is lower than the designed value (500V). Figure 8 shows the current and voltage waveforms of the first output (3.3V) rectifier diode. The maximum reverse voltage of this diode was calculated as 25V in Fig. 8 and the measured value is 32V and figure 9 is to show efficiency of designed flyback.

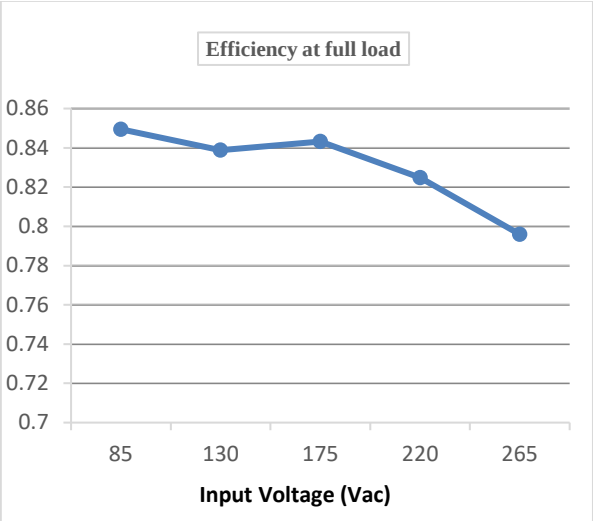

Figure 9. Simulated efficiency at full load

4. RESULTS

In this study, the design of a multiple output flyback converter circuit has been simulated in pspice environments. Firstly, the number of outputs, the output voltages and corresponding currents for the design have been identified. Secondly, components of proposed converters' power stage have been calculated. Besides, the simulation study has been carried out using eight-winding mutual inductance. Thirdly, control circuit has been designed using bode plot. At this point, a non-opto-coupler solution is to bring a significant improvement for both system performance and production cost. Lastly, it has been shown changing of output voltages at both input varieties and load changes. Importance of this paper is that all components used in simulation have nonlinear and proposed eight windings transformer is to include mutual inductance between each of windings. Mutual inductance is to occur slightly changings at output voltages. When flyback converter has been designed in a good way, it is shouldn't be forgotten effect of mutual inductance.

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